REMARKS

Claims 1-20 are pending and were rejected. No claims are being amended.

1. Rejections Under 35 U.S.C. § 103(a) and 35 U.S.C. § 102(b)

In the Office Action, at page 2, claims 1-20 stand rejected under 35 U.S.C. §103(a) as allegedly unpatentable over *Cavanna et al.*, (U.S. Patent 6,208,703), hereinafter *Cavanna*, in view of *Holm et al.*, (U.S. Patent 6,687,255), hereinafter *Holm*. It is well established at law that, for a proper 35 U.S.C. §103 rejection of a claim as being obvious based upon a combination of references, the cited combination of references must disclose, teach, or suggest, either implicitly or explicitly, all elements/features/steps of the claim at issue. See, *e.g.*, *In Re Dow Chemical*, 5 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1988), and *In re Keller*, 208 U.S.P.Q. 871, 881 (C.C.P.A. 1981).

In the Office Action, at page 6, claims 15-20 stand rejected under 35 U.S.C. §102(b) as allegedly unpatentable over *Cavanna*. For a proper rejection of a claim under 35 U.S.C. Section 102, the cited reference must disclose all elements/features/steps of the claim. See, *e.g.*, *E.I. du Pont de Nemours & Co. v. Phillips Petroleum Co.*, 849 F.2d 1430, 7 USPQ2d 1129 (Fed. Cir. 1988).

The applicant respectfully disagrees that *Cavanna* and *Holm*, singly or in any motivated combination is obvious over the present invention, and further disagrees that *Cavanna* by itself anticipates the present invention. The applicant successfully traverses the rejections of claims 1-20 over the cited prior art in the discussion that follows, and herewith requests that claims 1-20 be allowed as originally submitted.

A. Independent Claims 1 and 15

Claims 1 and 15 are allowable for at least the reasons that the proposed combination of *Cavanna* in view of *Holm* does not disclose, teach, or suggest several elements recited in claim 1 and that *Cavanna*, by itself, does not anticipate each of the elements recited in claim 15.

i. Cavanna's pointers do not control the address in a storage buffer

Claims 1 and 15 in the present application recite, *inter alia*, a "write pointer register connected to the storage buffer circuit ... to control the storage location at which data is written into the storage buffer circuit." By way of a non-limiting embodiment, the relationship is shown in FIG. 5 of the present application where the write pointer 92 is connected to the storage buffer circuit (FIFO) 60. The write pointer/storage buffer relationship is described in other non-limiting embodiments in the present application at paragraph [0047] and further revealed in FIGS. 4 and 6, which show the write pointer (wrptr) cyclically addressing locations in the FIFO.

Cavanna does not teach or suggest any write pointer register that controls the storage location at which data is written into a storage buffer circuit. Cavanna shows a write pointer flip-flop 41, but the only output of that flip-flop is directed to a synchronizer flip-flop 46, which is not a storage buffer circuit. Cavanna does show a 4-bit register 55, but that register 55 simply is not controlled by the write pointer flip-flop. The only connection between the flip-flop 41 and the register 55 is that they share inputs from an AND gate 45, a reset line NotWrtRST 59, and a clock input WrtCLK. Sharing inputs in no way implies that the flip-flop controls the register 55.

Even if the output of the write pointer flip-flop 41were somehow connected to control the register 55, Cavanna still does not satisfy the claim language, because the flip-flop does not control which of plural storage locations at which data is written into a storage buffer circuit. That is because the 4-bit register 55 of Cavanna includes only a single storage location to which data from a data line 60 is stored. That is, every time that data is loaded into the register 55, all 4 bits of the single storage location of the register 55 are written to. Thus, there is no need or use for a write pointer register to control the storage location at which data is written into the register 55.

In addition to a write pointer register, claims 1 and 15 in the present application recite, *inter alia*, a "read pointer register connected to the storage buffer circuit ... to control the storage location from which data is read from the storage buffer circuit." By way of a non-limiting embodiment, FIG. 5 of the present application shows the read pointer 94 and its

connection to the storage buffer circuit (FIFO) 60. The read pointer/storage buffer relationship is described in other non-limiting embodiments in the present application at paragraph [0047] and further revealed in FIGS. 4 and 6 where the read pointer (rdptr) is shown cyclically addressing locations in the FIFO. As described above with respect to the write pointer register language, there is no fair reading of *Cavanna* that discloses, teaches, or suggests any such relationship, and therefore, claims 1 and 15 are neither anticipated nor rendered obvious by the prior art.

ii. Cavanna Does Not Have Logic to *Increment* a Count Held in a Write Pointer Register

Claims 1 and 15 recite read and write control logic that will "increment the count held" in the read and write "pointer registers" respectively.

The cited prior art does not teach or suggest holding counts in read and write pointer registers, respectively. Cavanna shows respective write and read pointer flip-flops 41, 51 (Fig. 2), but those flip-flops do not hold any counts. The write and read pointer flip-flops are T flip-flops. It is known in the art that T flip-flops merely toggle their outputs when the signal at pin T is asserted (and the flip-flop is clocked), and that T flip-flops do not store data. As such, the flip-flops 41, 51 cannot hold any counts. For example, if the current output of the T flip-flop is 1, then asserting the T input changes the output to 0; conversely if the current output is 0 and the T input is asserted, then the output changes to 1. As such, the T flip-flop does not hold any count – it's output simply toggles between 1 and 0 when the T input is asserted.

One of the many significant differences between the present application and the prior art is that the circuit of Figure 2 of Cavanna is a "single stage FIFO synchronizer" (col. 6, lines 10-38). The importance of a "single stage FIFO synchronizer" is that Cavanna discloses a FIFO synchronizer with only one storage location (*i.e.*, one single stage). It is evident to those skilled in the art that a single stage FIFO synchronizer does not require "pointer registers" as recited in claims 1 and 15 because the writing and reading circuits will always direct data into or from the one single storage location. Accordingly, Cavanna can clock data through his invention, but he does not have read and write pointer registers in which he can "increment the count held."

The Office Action states that these elements of the present application are represented in FIG. 2 of *Cavanna* as AND2 gates 45 and 50.

iii. Cavanna's Logic Does Not Control Writing Data To Successive Locations

Claims 1 and 15 in the present application recite, *inter alia*, that "write control logic in the storage buffer control circuit is adapted to control the write pointer register such that data received at the data input of the associated storage buffer circuit is written into successive storage locations of the storage buffer circuit as the data is received so long as the storage locations are not all full." The *Cavanna* reference does not anticipate these limitations, nor are they obvious. Unlike the present application, the *Cavanna* reference does not have a write pointer register that directs where received data will be written, and in fact, Cavanna's single stage FIFO synchronizer does not have "successive storage locations." Although the prior art does show a NotFull 56 signal (*see Cavanna*, FIG. 2), this signal is only an indicator that the single data element written into the single storage location has not yet been read by the target. Accordingly, because these features of claims 1 and 15 are not found in the prior art, claims 1 and 15 are further allowable.

iv. Cavanna's Storage Buffer Does Not Have A Plurality Of Storage Locations

The Office Action implies that the "storage buffer circuit" recited in claims 1 and 15 of the present application is represented in FIG. 2 of *Cavanna* as Register 55; a 4-bit wide register. Cavanna's specification, in several places, describes FIG. 2 as a "single stage FIFO synchronizer." (Col. 6, lines 10-38). As described above, a "single stage FIFO synchronizer" is only capable of storing one data element at a time. This description of a "single stage FIFO synchronizer" is supported in the *Cavanna* specification, which recites that the invention shown in FIG. 2 is only capable of transferring data, "one transition per handshake cycle." (Col. 6, lines 36-38). It is recognized by those in the art that by stating "one transition per handshake cycle," Cavanna means that his invention can only pass a single data element on each clock cycle. Because

Cavanna's invention has only a single stage FIFO synchronizer, it necessarily has only one storage location.

In contrast, claims 1 and 15 in the present application recite the limitation that the storage buffer circuit must contain a "plurality of storage locations." Support for the plurality of storage locations in the FIFO is evident in the non-limiting embodiments shown FIGS. 3, 4, and 6 of the present application. Because *Cavanna* fails to disclose, teach or suggest the limitation of "plurality of storage locations" as found in claims 1 and 15, these claims are further allowable.

v. The *Holm* reference does not cure the deficiencies of *Cavanna*

Holm does not teach or suggest any of the claimed features discussed above that are missing from Cavanna. In particular, Holm does not teach or suggest any write or read pointer registers or any logic that controls such registers. Given that the Office Action referenced *Holm* only for the feature of not reading storage locations until after a predetermined time delay, it seems unnecessary to address Holm further.

For the foregoing reasons, claims 1 and 15 are not anticipated or rendered obvious by the cited prior art.

B. Dependent Claims 2 – 14 and 16 – 20

Because independent claims 1 and 15 are allowable over the cited art of record, dependent claims 2-14 (which depend from independent claim 1) and dependent claims 16-20 (which depend from claim 15) are allowable as a matter of law for at least the reason that dependent claims 2-14 contain each of the elements of independent claim 1 and dependent claims 16-20 contain each of the elements of independent claim 15. See, *e.g.*, *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988). Accordingly, the applicant respectfully requests that the rejections to dependent claims 2-14 and dependent claims 16-20 be withdrawn.

2. Conclusion

Overall, none of the references singly or in any motivated combination disclose, teach, or suggest what is recited in the independent claims. Further, in light of the remarks, the applicant respectfully submits that all objections and/or rejections have been traversed, rendered moot, and/or accommodated, and that pending claims 1-20 are in condition for allowance. The applicant, therefore, respectfully requests that the Examiner reconsider this application and timely allow all pending claims. The Examiner is encouraged to contact the undersigned attorney by telephone to discuss the above and any other distinctions between the claims and the applied references, if desired. If the Examiner notes any informalities in the claims, he is further encouraged to contact the undersigned attorney by telephone to expediently correct such informalities.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

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